AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (previously presented) A memory system comprising:

a plurality of nonvolatile memory chips each having a plurality of memory banks which can perform a memory operation independent of each other; and

a memory controller which can control to individually access each of said nonvolatile memory chips,

wherein in the case of giving a write instruction designating an address to a nonvolatile memory chip and, after that, giving a write instruction designating another address to said nonvolatile memory chip, said memory controller can selectively instruct a simultaneous writing operation or an interleave writing operation, and

wherein after giving a write instruction designating said another address to one of said plurality of nonvolatile memory chips, said memory controller can give a write instruction designating further another address to another nonvolatile memory chip in said plurality of nonvolatile memory chips.

2. (original) The memory system according to claim 1, wherein said simultaneous writing operation is a writing operation started at the same timing on the plurality of memory banks after serial plural instructions of the writing operation designating the memory banks, and

wherein said interleave writing operation is a writing operation of starting a new writing operation in response to a write instruction designating another memory bank during a writing operation which has already started.

3. (original) The memory system according to claim 2, wherein said memory controller discriminates between an instruction of said simultaneous writing operation and an instruction of said interleave writing operation in accordance with a kind of a command code which accompanies write address information and write data information and instructs a writing operation.

4. (original) The memory system according to claim 1, wherein each of said nonvolatile memory chips has a chip select terminal and other plural access terminals, and

wherein said memory controller has a chip select signal output terminal individually coupled to said chip select terminal of each of the nonvolatile memory chips and a

plurality of access information terminals commonly coupled to said access terminals of each of said nonvolatile memory chips.

5. (previously presented) A memory system comprising:

a plurality of nonvolatile memory chips each having a plurality of memory banks which can perform a memory operation independent of each other; and

a memory controller which can control to individually access each of said plurality of nonvolatile memory chips,

wherein said memory controller can sequentially instruct interleave writing or simultaneous writing on the memory banks in each of said nonvolatile memory chips.

6. (original) The memory system according to claim 5, wherein said interleave writing instruction is a writing operation instruction for starting a new writing operation in response to a write instruction designating another memory bank during a writing operation already started.

7. (original) A memory system comprising:

a plurality of nonvolatile memory chips each having a plurality of memory banks which can perform a memory operation independent of each other; and

a memory controller which can control to individually access each of said nonvolatile memory chips,

wherein said memory controller can sequentially instruct simultaneous writing on the memory banks in each of said nonvolatile memory chips.

8. (original) The memory system according to claim 7, wherein said simultaneous writing instruction is a writing operation instruction for starting the writing operation at the same timing on a plurality of memory banks after serial plural instructions of the writing operation designating the memory banks.

9. (original) A memory system comprising: a plurality of flash memory chips each having a plurality of memory banks which can perform a memory operation independent of each other;

a memory controller which can control to individually access each of said plurality of flash memory chips; and

an SRAM coupled to said memory controller,

wherein said SRAM can temporarily store write data to the flash memory chips, and

wherein said memory controller can select an instruction of sequentially performing interleave writing on

the memory banks in each of the flash memory chips or an instruction of sequentially performing simultaneous writing the memory banks in each of the flash memory chips.

10. (original) The memory system according to claim 9,

wherein said interleave write instruction is a writing operation instruction for starting a new writing operation in response to a write instruction designating another memory bank during a writing operation which has already started, and

wherein said simultaneous write instruction is a writing operation instruction for starting the writing operation at the same timing on the plurality of memory banks after serial plural instructions of the writing operation designating memory banks.

11. (previously presented) A memory system comprising:

a plurality of flash memory chips each having a plurality of memory banks which can perform a memory operation independent of each other; and

a memory controller which can control to access said flash memory chip by using an access command,

wherein said memory controller can select either a first control of outputting a first command code, address information of a memory bank subsequent to the first command code, and a second command code subsequent to the address information of the memory bank and making a memory bank in a flash memory chip designated by said address information start a memory operation every input of the second command code, or a second control of outputting a first command code, address information of a memory bank in a flash memory chip subsequent to the first command code, a third command code subsequent to the address information of the memory bank, address information of a memory bank in a flash memory chip subsequent to the third command code, and a second command code subsequent to the address information of the memory bank, and making a plurality of memory banks designated by a plurality of pieces of address information separated by said third command between said first command code and said second command code simultaneously start a memory operation in response to input of the second command code, and allow the plurality of flash memory chips perform the memory operation in a serial manner.

12. (original) The memory system according to claim 11, wherein said first command code is a command code indicative of a kind of the writing operation, the second

command code is a command code for instructing start of the writing operation, and the third command code is a command code indicating that address information follows.

13. (previously presented) A memory card comprising, on a card board:

an external terminal;

an external interface circuit coupled to said external terminal;

a memory controller coupled to said external interface circuit; and

a plurality of flash memory chips each subjected to an access control by said memory controller,

wherein said flash memory chip has a plurality of memory banks which can perform a memory operation independent of each other,

wherein in the case of giving a write instruction designating an address to a flash memory chip and, after that, giving a write instruction designating another address to said flash memory chip, said memory controller can selectively instruct a simultaneous writing operation or an interleave writing operation, and

wherein, after giving a write instruction designating said another address to one of said plurality of flash memory chips, said memory controller can give a write

instruction designating further another address to another flash memory chip in said plurality of flash memory chips.

14. (original) The memory card according to claim 13,

wherein said simultaneous writing operation is a writing operation started at the same timing on a plurality of memory banks after serial plural instructions of the writing operation designating the memory banks, and

wherein said interleave writing operation is a writing operation for starting a new writing operation in response to a write instruction designating another memory bank during a writing operation which has already started.

15. (original) The memory card according to claim 14, wherein said memory controller discriminates between an instruction of said simultaneous writing operation and an instruction of said interleave writing operation in accordance with a kind of a command code which accompanies write address information and write data information and instructs a writing operation.

16. (original) The memory card according to claim 15, further comprising an SRAM coupled to said memory controller,

wherein said SRAM can temporarily store write data to a flash memory chip.

17. (original) The memory card according to claim 13, wherein said external terminals include a 1-bit data input/output terminal, a 1-bit command terminal, a power source voltage terminal, a circuit's ground voltage terminal, and a clock terminal.

18. (previously presented) A nonvolatile semiconductor memory device comprising:

a memory controller; and

a plurality of nonvolatile memories,

wherein said memory controller issues a write instruction command including address information indicative of an address in which information is to be written to said plurality of nonvolatile memories,

wherein said nonvolatile memory has a plurality of storage regions which are separated by addresses and can be accessed in parallel with another storage region, and

wherein said memory controller simultaneously issues write instruction commands designating different storage regions and, after that, can perform simultaneous writing for starting a writing operation on said designated plurality of memory regions at the same timing, on a plurality of nonvolatile memories in a serial manner.

19. (original) The nonvolatile semiconductor memory device according to claim 18,

wherein said nonvolatile memory has a plurality of memory cells, and

wherein a writing operation of said nonvolatile memory is performed by selecting a group of memory cells in accordance with an address instructed by said write instruction command and changing a threshold voltage according to information to be written into each of the selected memory cells.

20. (original) The nonvolatile semiconductor memory device according to claim 18,

wherein the writing operation of said nonvolatile memory includes a first operation for changing the threshold voltage of a memory cell, and a second operation for confirming whether the threshold voltage of each of the memory cells has changed to a threshold voltage corresponding to said information to be written, and

wherein in the case where the threshold voltage of at least one memory cell has not changed to a threshold voltage corresponding to the information to be written after said second operation, said first operation is performed.

21. (original) The nonvolatile semiconductor memory device according to claim 20, wherein in said plurality of memory cells, a threshold voltage included in a threshold voltage distribution corresponding to information to be written out of three or more threshold voltage distributions is set.

Claims 22-32 (cancelled).